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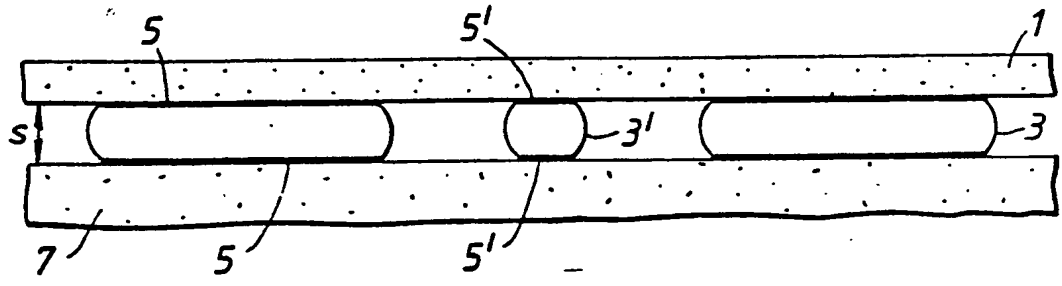
(54) Title: MANUFACTURE OF A HYBRID ELECTRONIC OR OPTICAL DEVICE



(57) Abstract

In a flip chip bonding operation, a chip (1) is required to be accurately aligned over a pattern of electrical connector pads (5) on a substrate body (7). Electrical connections between the chip (1) and the pads (5) on the body are formed by solder bumps (3) which are fused to make the connections permanent. The method of the invention provides means for accurately aligning the chip (1) by using surface tension forces which arise in the solder portions when these are fused. A solder bump (3) having a diameter of at least 40 micrometres provides adequate force for the alignment and it allows solder bonds having a lesser diameter to be accurately aligned between the two components. The method can also be used to align the components of an optical device.

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MANUFACTURE OF A HYBRID ELECTRONIC OR OPTICAL DEVICE

The present invention concerns the manufacture of a hybrid electronic or optical device and in particular to a method of alignment capable of being employed in the manufacture of for example solder bonded hybrid electronic devices.

The fabrication of certain types of flip-chip bonded hybrid electronic devices, for example 2-dimensional thermal detector arrays and certain electro-optic devices, can require the use of very small solder bonds in the flip-chip structure. For example solder bond diameters as low as 10 to 20 micrometres are envisaged in particular devices now under development. The successful alignment and bonding of flip-chip devices with such small solder bonds requires extremely accurate mechanical alignment of the two components. This can present practical problems, both in providing suitable alignment features on the chip accurately registered to the array of solder bonds which are, of course, hidden beneath the chip during bonding, and in achieving the required alignment accuracy in the bonding equipment itself. In other devices the accurate alignment of micro-optical devices to an integrated optics substrate is required.

Flip-chip bonding is now a well established technique. In this technique it is conventional to provide an

electronic semiconductor chip and a co- operative substrate with mirror image patterns of bonding pads. Equi-sized solder bumps are deposited on either the chip or substrate, or in some cases upon both, the chip is then flipped over and registered above the substrate, and the solder reflowed. Provided the chip and substrate have been registered within tolerable accuracy, the two are then self-aligned.

The natural self-aligning nature of the flip-chip solder bonding process is effective provided that the mass of the chip component is not excessive, and provided good solder wetting is assured. The self-alignment process will come into play provided the solder bump on the chip (after it collapses on first melting to give a shape close to that of a truncated sphere with a contact angle equal to that of the non-wettable area of the substrate) contacts and overlaps the wettable pad on the substrate. This, to a first approximation, requires that the two components be aligned to a better than one wettable pad diameter distance. A practical lower limit on alignment of flip-chip devices employing a single solder bump size has been found to be at about a 40 micrometre solder bump and pad diameter. A more useful figure for a rapid alignment and solder bonding cycle on the manually controlled precision alignment equipment employed is 70 micrometres diameter. An automated pitch-and-place

method for placing and aligning flip-chip components would probably require a still larger bump and pad diameter for example 100-150 micrometres. Practical problems may arise when solder bump and pad diameters below about 40 micrometres are required.

The present invention was devised to provide a solution to the problems aforesaid.

There is herein provided a method for achieving natural and highly accurate alignment of small diameter solder bonds in a flip-chip device, for aligning small optical components on an integrated optic substrate.

In accordance with the present invention there is provided a method of manufacture of a hybrid, solder-bonded electronic device where a substrate portion of the device is required to have a chip portion electronically connected thereto with confronting connection pads on the two portions being joined by solder bonds, the method comprising the steps of providing solder wettable contact pads on the substrate portion in a required pattern for forming the neccesary electrical connections, providing a corresponding pattern on the chip portion, depositing a separate solder portion onto each respective contact pad of a least one of the substrate portion and the chip portion, fusing said solder portions so as to form a solder bump from each solder portion on its contact pad, positioning said chip portion

on said substrate portion so that each said solder bump is brought near to a corresponding solder wettable contact pad, heating said substrate and chip portions so that the said solder bumps became fused, the consequent flowing of the said solder portions acting to wet the respective confronting contact pads to form separate solder joints, surface tension forces then causing adjustment of the position of the said chip with respect to said substrate such that an accurate alignment of said confronting patterns of pads is effected, cooling the fused portions to form solder joints connecting the patterns of pads thereby uniting the chip portion to said substrate portion and establishing the required electrical connections.

The said solder bumps may include at least one bump of diameter between 40 and 150 micrometres. The said solder bumps may include at least one bump of diameter 70 micrometres or greater. The solder bumps may include two or more bumps of diameter 40 micrometres or greater, with further bumps of a smaller diameter.

According to a further aspect, the invention comprises a method of aligning co-operating areas of confronting parts of an electronic or optical device, the method comprising the steps of providing solder wettable contact pads on each portion onto each respective contact pad of at least one of the said confronting parts, fusing

said solder portion so as to form a solder bump from each solder portion on its contact pad, positioning the confronting parts together such that each solder bump is brought near to a corresponding solder wettable contact pad, heating said confronting parts such that the said solder bumps become fused, the consequent flowing of the said solder portions acting to wet the respective confronting contact pads to form separate solder joints, surface tension forces then causing adjustment of the position of one confronting part with respect to the other part such that an accurate alignment of said co-operating areas is effected, cooling the fused portions to form solder joints connecting the contact pads thus joining the confronting parts and providing accurate alignment of the said co-operating areas.

The invention also comprises an electronic or optical device when manufactured by the disclosed alignment method.

The solution thus is to provide a number of relatively large diameter solder bumps on a chip or substrate, whose function is to provide surface tension self-alignment of an array of smaller solder bumps or other cooperative device features. The large bumps extend the alignment tolerances during the bonding operation and are designed to physically contact the substrate first so as to align the chip to the substrate prior to the

formation of any smaller bonds.

The 'major' and 'minor' solder bumps in the array on the chip are generally defined by applying solder over an area larger than that of the wettable metallisation and then reflowing (or fusing) the solder to form the bumps.

The heights of the major and minor bumps may be controlled by varying the dewetting ratio (the solder deposition area to wettable pad area ratio) in the appropriate manner to ensure that the final bonds, once made, are of equal equilibrium height, whilst, prior to bonding, the major bumps are the greater in height.

The solder itself may be applied by electro deposition or by a thermal deposition technique, for example electron beam deposition using a thick resist mask. Thermal deposition is the preferred process.

For low mass chips the mass acting on each solder bond in the array may generally be neglected, and thus, for the usual case of equal wettable pad diameters on chip and substrate, the solder bond shape closely approximates, for circular pads, to a truncated sphere. The use of circular pad geometries is preferred, for this allows a simple calculation of solder bump and joint dimensions, de-wet ratios, etc. to be made for different device configurations.

BRIEF INTRODUCTION OF THE DRAWINGS

In the drawings accompanying this specification:-

Figure 1 is a schematic view of a flip-chip and substrate, showing solder bump and bonding pad patterns;

Figures 2(a) to (d) are cross-section at views of a flip-chip and substrate at successive stages during a bonding process;

Figures 3 and 4 are cross-sectional views showing the relative size of solder bumps and bonding pads as applied to align small diameter solder bonds for a flip-chip device; and,

Figure 5 is a cross-sectional view showing the relative size of solder bonds and device features as applied to align small optical components on an integrated optic substrate.

DESCRIPTION OF EMBODIMENTS

So that the invention may be better understood, details of embodiments of this invention will now be described, by way of example only, and with particular reference to the accompanying drawings.

A schematic diagram of a conventional 'flip-chip' device structure is shown in Figure 1. A device chip 1, which possesses an array of solder bumps 3 defined on solder wettable metallisation pads at appropriate points on the device, is flipped over to mate with a corresponding (mirror-imaged) array of solderable metal pads 5 on substrate 7 (in general solder may be present on either or both components, the choice depending upon the

particular device and materials of interest). The chip 1 may be, for example, a thermal detector array, an optoelectronic device, a silicon or gallium arsenide circuit or a thin film circuit or component. The substrate 7 may be, for example, a thick or thin film circuit, or a second integrated circuit. The flip-chip hybrid device may comprise for example a 16x16 element pyroelectric detector array interfaced to a charge coupled device silicon integrated circuit device, which acts as a compact, uncooled solid state thermal imaging device. The flip-chip structure and process allows very large numbers of electrical connections between two components or devices to be made in a highly space-efficient manner in a single, simple bonding operation. For example in a recent flip-chip bonded test device more than a thousand solder bonds were successfully made in a single operation on a chip 3.5mm square. Bonding is achieved by placing the components in contact, with the solder bumps 3 on the chip 1 overlapping the solder wettable pads 5 on the substrate 7, and then raising the assembly above the liquidus temperature of the particular solder employed. The solder then melts and wets onto the wettable pads. The high surface tension of the solder (200-600 $mJ.m^{-2}$ depending on composition and environment) then acts to align the components, as illustrated in Figures 2(a) to (d).

As can be seen from these figures, provided the solder bump 3 is in close proximity to the bonding pad 5, the solder, on melting, touches the pad 5-Fig.2(b). Surface tension effects then cause the solder to wet the remaining portion of the pad 5 and to pull the chip 1 in a direction towards alignment-Fig.2(c), until ultimately accurate alignment is achieved-Fig.2(d).

A variety of solder compositions and wettable metallisation formulations may be employed. The 95 wt% lead : 5 wt% tin solder (solidus 310°C, liquidus 314°C) and the 37 wt% lead : 63 wt% tin solder (eutectic composition temperature 183°C) are commonly employed in flip-chip devices. Wettable metallisation formulations are invariably multi-layer metallic coatings, comprising an adhesion and diffusion barrier layer (for example chromium), a solderable layer (for example nickel or copper), and a tarnish prevention layer (for example gold). If copper is employed as the solderable metal then it is important to ensure that there is a region of alloying between the barrier layer and the copper to prevent total dissolution of the copper when soldering, which would then result in de-wetting. The wettable pads 5 may be rectangular, square or circular, the latter geometry greatly simplifying the calculation of solder bump and bond geometries. This surface tension alignment process is herein utilised to align smaller scale solder

bonds or small device features as shown in Figures 3 and 4 respectively.

As shown in Figures 3 and 4,a pattern of bonding pads 5, 5' is defined upon the surface of a chip 1. A mirror image pattern is likewise defined on the surface of a supportive substrate 7. A particular feature of these patterns is that they each include relatively large size key pads 5 compared with those pads 5' for which alignment is required. The smaller size pads 5' are of diameter 2x', typically less than 40 micrometres. The key pads 5 are chosen to be of a size facilitating registration, typically in the range 40 micrometres to 150 micrometres diameter (corresponding to diameter 2x).

Solder has been deposited upon one of the pad patterns and melted to form bumps. The amount of solder deposited has been regulated to ensure that the height h of each key pad solder bump 3 is somewhat in excess of the height h' of the smaller scale bumps 3'. This height difference is represented by the symbol 'z' in Figure 3. This ensures that when the chip 1 is flipped over and located in register upon the substrate 7, contact is first made between the key pads 5 and the key solder bumps 3. Initially, the target pads 5' and the target solder bumps 3' are held out of contact. During subsequent solder reflow or fusion, the target pads 5' and bumps 3' are pulled into accurate alignment by surface tension forces.

An example of the foregoing flip-chip structure is given below:-

SOLDER BUMP GEOMETRIES FOR COMPATIBLE 10 & 70 MICRON DIA.BONDS

	MINOR	MAJOR
WETTABLE RADIUS (x',x) :	5	35 micrometres
DEPOSITION RADIUS (-) :	10	52.429 "
REFLOW HEIGHT (h',h) :	12.698	20.197 "
BOND HEIGHT (S) :	11.036	11.036 "
CONTACT ANGLE (0) :	155.628°	107.502°

SOLDER APPLICATION THICKNESS :	5.000 "
DIFFERENCE IN REFLOW HEIGHTS (z) :	7.499 "
DIFFERENCE IN MAJOR BOND TO MINOR REFLOW :	1.662 "
DIFFERENCE IN BOND HEIGHTS :	-0.000 "

The technique described may be used not only for aligning small scale size solder bumps, but also for aligning optical components. As shown in Figure 5, two small size optic device features 9, 9' have been aligned. These are separated by a bond height S of 25 micrometres, using 100 micrometre diameter bonding pads and solder bumps with a reflow height h of about 40 micrometres.

The foregoing description of embodiments of the invention has been given by way of example only and a number of modifications may be made within the scope of the invention as defined in the appended claims. For

instance, it is not essential that the method of the invention should be restricted to align small components which are only electronic devices. The method could be used alternatively to align other small components such as integrated optical components, pyroelectric elements and the like.

CLAIMS

1. A method of manufacture of a hybrid, solder bonded electronic device where a substrate portion of the device is required to have a chip portion electrically connected thereto with confronting connection pads on the two portions being joined by solder bonds, the method comprising the steps of providing solder wettable contact pads on the substrate portion in a required pattern for forming the necessary electrical connections, providing a corresponding pattern on the chip portion, depositing a separate solder portion onto each respective contact pad of at least one of the substrate portion and the chip portion, fusing said solder portions so as to form a solder bump from each solder portion on its contact pad, positioning said chip portion on said substrate portion so that each said solder bump is brought near to a corresponding solder wettable contact pad, heating said substrate and chip portions so that the said solder bumps become fused, the consequent flowing of the said solder portions acting to wet the respective confronting contact pads to form separate solder joints, surface tension forces then causing adjustment of the position of the said chip with respect to said substrate such that an accurate alignment of said confronting patterns of pads is effected, cooling the fused portions to form solder joints

connecting the patterns of pads thereby uniting the chip portion to said substrate portion and establishing the required electrical connections.

2. A method as claimed in Claim 1, in which the said solder bumps include at least one bump of diameter between 40 and 150 micrometres.

3. A method as claimed in Claim 2, in which the said solder bumps include at least one bump of diameter 70 micrometres or greater.

4. A method as claimed in Claim 1 or 2, in which the said solder bumps include two or more bumps of diameter 40 micrometres or greater, with further bumps of a smaller diameter.

5. A method of aligning cooperating areas of confronting parts of an electronic or optical device the method comprising the steps of providing solder wettable contact pads on each of said confronting parts depositing a separate solder portion onto each respective contact pad of at least one of the said confronting parts, fusing said solder portion so as to form a solder bump from each solder portion on its contact pad, positioning the

confronting parts together such that each solder bump is brought near to a corresponding solder wettable contact pad, heating said confronting parts such that the said solder bumps became fused, the consequent flowing of the said solder portions acting to wet the respective confronting contact pads to form separate solder joints, surface tension forces then causing adjustment of the position of one confronting part with respect to the other part such that an accurate alignment of said cooperating areas is effected, cooling the fused portions to form solder joints connecting the contact pads thus joining the confronting parts and providing accurate alignment of the said cooperating areas.

6. A method of manufacture of an electronic or optical device substantially as hereinbefore described with reference to any one of Figures 1 to 4 of the accompanying drawings.

7. An electronic or optical device when manufactured by a method as claimed in any one of Claims 1 to 6.

8. An electronic or optical device substantially as hereinbefore described with reference to any one of Figures 2 to 5 of the accompanying drawings.

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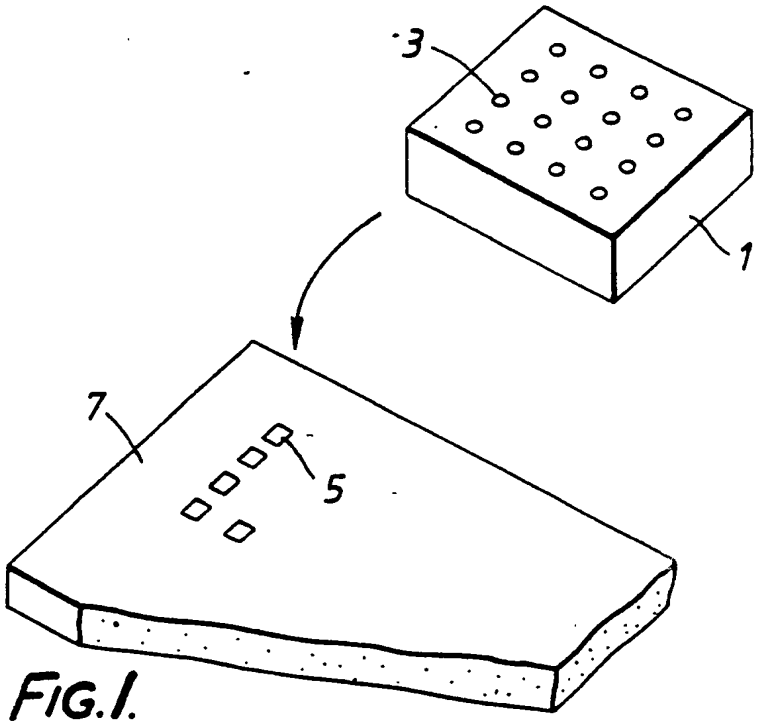

FIG. 1.

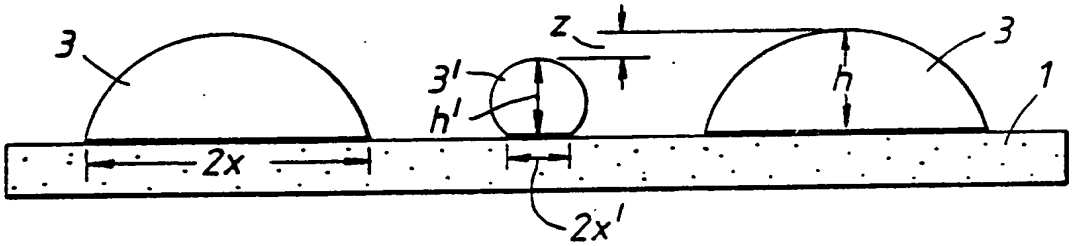

FIG. 3.

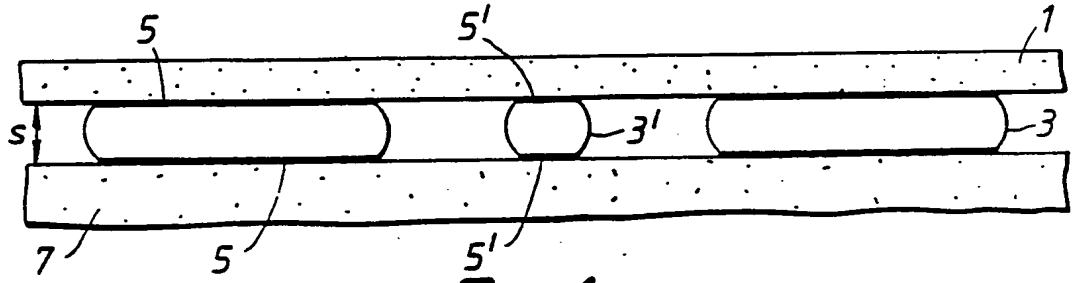

FIG. 4.

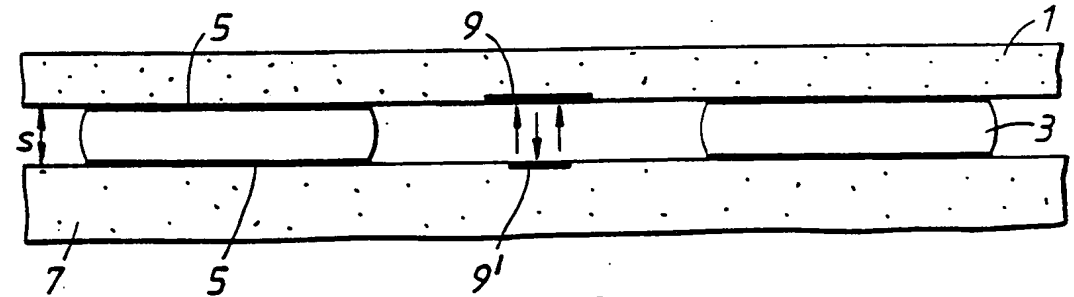

FIG. 5

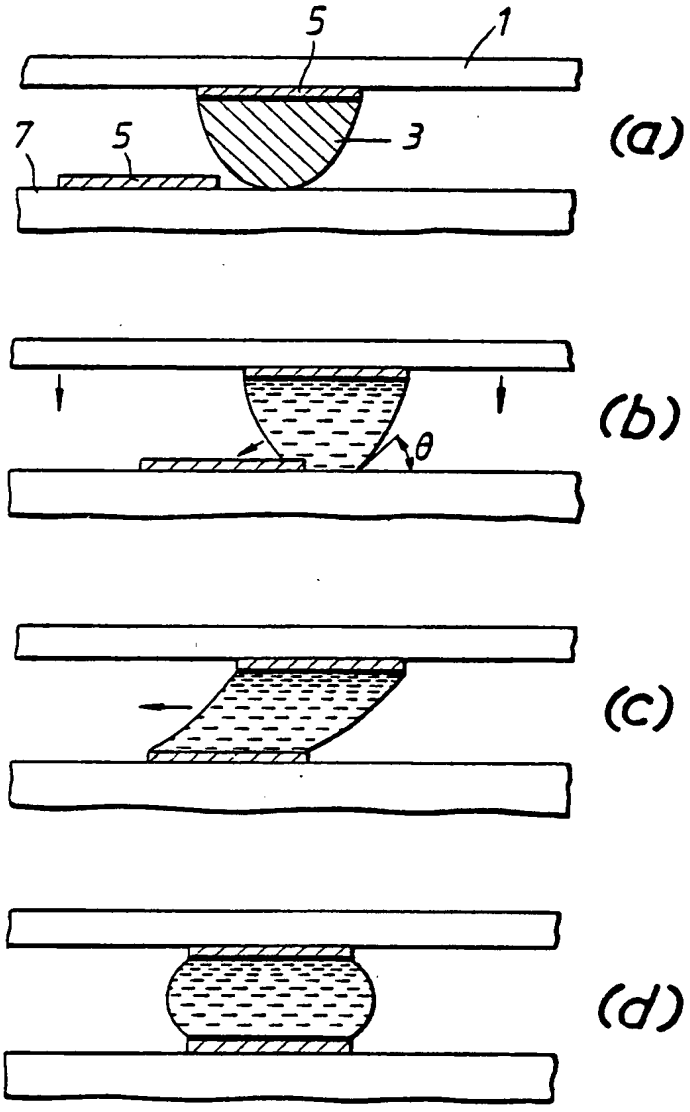

FIG.2.

INTERNATIONAL SEARCH REPORT

International Application No PCT/GB 86/00538

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[4]: H 01 L 21/60

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC[4]	H 01 L

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
X	GB, A, 2062963 (HITACHI) 28 May 1981, see abstract; page 2, lines 120-124; page 3, lines 6-9,86-91	1,7
A	--	2-6,8
X	US, A, 3997963 (IBM) 21 December 1976, see abstract; column 6, lines 51-65	1
A	--	5-8
A	EP, A, 0147576 (IBM) 10 July 1985, see abstract; page 1, lines 26-31	1,5-8
A	-- US, A, 3486223 (PHILCO) 30 December 1969, see column 3, lines 52-58	1,5-8
A	-- DE, A, 2909370 (CITIZEN WATCH) 20 September 1979, see claim 7	2,3
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* Special categories of cited documents: [10]

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
12th November 1986	11 DEC 1986
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	M. VAN MOL

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/GB 86/00538 (SA 14458)

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 18/11/86

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
GB-A- 2062963	28/05/81	None	
US-A- 3997963	21/12/76	US-A- 3893156 US-A- 4032058	01/07/75 28/06/77
EP-A- 0147576	10/07/85	JP-A- 60119737 US-A- 4545610	27/06/85 08/10/85
US-A- 3486223	30/12/69	None	
DE-A- 2909370	20/09/79	JP-A- 54121970	21/09/79